0 read request from L1 data cache

9 print contents and state of each valid cache line

Address #1; the cache is empty and there will be a read request to the memory and the state of that line will be exclusive.

0 read request from L1 data cache

9 print contents and state of each valid cache line

Address#1; to get a hit.

1 write request from L1 data cache

9 print contents and state of each valid cache line

Address#1; it will invalidate the other copies of the line in other caches. And change the line to modified state

0 read request from L1 data cache

9 print contents and state of each valid cache line

Address#1; it will read and don’t send any bus operations.

1 write request from L1 data cache

9 print contents and state of each valid cache line

Address#1; it will write to the line without putting anything on the bus

4 snooped read request

9 print contents and state of each valid cache line

Address#1; write back the line and put it in the shared state.

0 read request from L1 data cache

9 print contents and state of each valid cache line

Address#1; it will read since it is in the shared state.

4 snooped read request

9 print contents and state of each valid cache line

Address#1; the other CPU will forward the line.

6 snooped read with intent to modify

9 print contents and state of each valid cache line

Address#1; we should invalidate our copy.

1 write request from L1 data cache

9 print contents and state of each valid cache line

Address#1; we will sniff the line when the other CPU write back the line and then the line should be in the forward state.

6 snooped read with intent to modify

9 print contents and state of each valid cache line

Address#1; forward the line and then invalidate our copy.

0 read request from L1 data cache

9 print contents and state of each valid cache line

Address#1; sniff that line and put it in the forward state.

0 read request from L1 data cache

9 print contents and state of each valid cache line

Address#1: do nothing on bus put read from the cache.

1 write request from L1 data cache

9 print contents and state of each valid cache line

Address#1; change that line to modified state and then send an invalidate signal

4 snooped read request

9 print contents and state of each valid cache line

Address#1; write back that line so the requesting CPU will sniff that and change the line to the shared state.

1 write request from L1 data cache

9 print contents and state of each valid cache line

Address#1; invalidate other copies and then put the line in the modified state.

6 snooped read with intent to modify

9 print contents and state of each valid cache line

Address#1: error.

0 read request from L1 data cache

9 print contents and state of each valid cache line

Address#2: read it from the memory and put it to the exclusive state.

4 snooped read request

9 print contents and state of each valid cache line

Address#2; forward the line and put it in the shared state.

3 snooped invalidate command

9 print contents and state of each valid cache line

Address#2; invalidate your copy.

0 read request from L1 data cache

9 print contents and state of each valid cache line

Address#3; new data is coming save it and put it in the exclusive state.

6 snooped read with intent to modify

9 print contents and state of each valid cache line

Address#3; error.

0 read request from L1 data cache

9 print contents and state of each valid cache line

Address#3; give it the data.

4 snooped read request

9 print contents and state of each valid cache line

Address#3; forward the line and put the line in the shared state.

6 snooped read with intent to modify

9 print contents and state of each valid cache line

Address#3; invalidate your copy

0 read request from L1 data cache

9 print contents and state of each valid cache line

Address#3; sniff the line from the other CPU and put the line in the forward state.

6 snooped read with intent to modify

9 print contents and state of each valid cache line

Address#3; invalidate your copy.

0 read request from L1 data cache

9 print contents and state of each valid cache line

Address#3; sniff the line from the other CPU and put the line in the forward state.

3 snooped invalidate command

9 print contents and state of each valid cache line Address#3; invalidate your copy.